INSTRUCTION DATA 050376B

RFL Industries, Inc., Boonton, New Jersey 07005

RFL Models 66 LD and 66 LD/CD 8-POINT LAMP DRIVER and 4-POINT CHANGE DETECT and LAMP DRIVER

DESCRIPTION

Models 66 LD and 66 LD/CD are two of the RFL Series 66 TDMS plug-in modules. They have the capability to drive either a single lamp for on-off indication, or the cards can drive complementary lamps for a red-green type of indication. Model 66 LD/CD has change of state detectors and can cause the respective lamp to flash if unauthorized status changes occur at any of the four input lines, while Model 66 LD has provision for external flash control on each of its eight inputs. Blank and lamp-test capability are also included on each card.

SPECIFICATIONS

Output Drive Current: 160 mA max. each output.

Output Transistor Breakdown Voltage: 40 V.

Temperature Range: -30^{o}C to $+70^{o}$C.

Power: Model 66 LD: 11-13 Vdc @ 23 mA + lamp current.
Model 66 LD/CD: 11-13 Vdc @ 14 mA + lamp current.

Size: One standard one-half-inch module increment in an RFL Series 68 Chassis.

CONNECTIONS, PROGRAMMING & THEORY

These modules contain CMOS logic circuits and special handling precautions should be observed. Refer to "CMOS Handling Precautions", RFL Document 12175.

All unused input terminals or unused inputs to IC's must be returned to +V or common.

The discussion in the following paragraphs will concentrate on Point 1 of the 66 LD/CD. A clear understanding of the 66 LD should result when the schematics are compared.

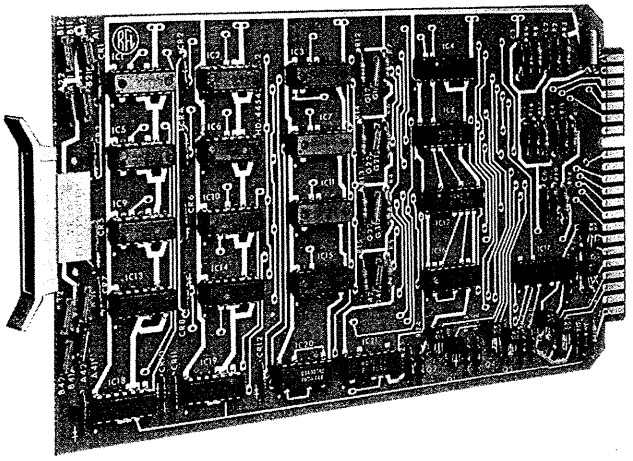


Figure 1. Model 66 LD/CD.

Lamps which require less than 160 mA are connected between a positive voltage and the open collector output terminals. The positive voltage source can be different from the twelve-volt supply that is used to power the CMOS logic.

Referring to the schematic, Figure 5, a logic 1 at Terminal 3 causes IC8A-3 to drop low. Since both inputs to IC3B are high, its output will also be low. Two lows at the input to IC20C force IC20C-10 high and turn on Q1 through gate IC21D and R24. Q2 is held off because the inverter output IC12F was at a logic 1 which maintains a 0 at IC20D-11. Thus a logic 1 at input Terminal 3 will light a lamp connected to the PT 1 "1" LAMP terminal, and likewise, a 0 at the PT 1 STATUS input will light a lamp connected to the output PT 1 "0" LAMP terminal.

A logic 1 at Terminal 13, ALL BLANK BUSS is inverted by IC12D to force IC3B-4 high, which in turn makes IC20C-10 and IC20D-11 both low and removes transistor base drive. A logic high at the LAMP TEST BUSS, Terminal 6, will cause all the lamps to turn on regardless of their status. IC21D-11 and IC21C-10 will both be at logic highs to provide base current into Q1 and Q2. Lamp testing takes priority over blanking.

The FLASH BUSS input should be connected to a source of low frequency squarewaves such as is available from the Model 66 ALRT card. When a change of status takes place there will be a logic 1 at Terminal E, PT 1 CHGD, and IC3C-10 will be oscillating. Jumper G11 should be installed if complementary red-green lamps are wired at Q1 and Q2. The alternating zeros at IC3B-5 will cause periodic blanking of the red or green lamp, whichever one was on. If only one output from either Q1 or Q2 is to be used then Jumper G12 should be installed. The square-wave signal at IC8A-1, coming from FS, alternately turns on Q1 and Q2. In this manner a lamp which would otherwise be steadily on is periodically turned off; while a lamp which would otherwise be off, is periodically turned on.

LAMP COMMON at Terminals 22 and Z should have a return path in the external wiring to COM at Terminals 1 and A. The wiring should be planned, however, to minimize the effect that high surge currents in the LAMP COMMON buss could have upon the logic.

If a 0-to-1 transition of the point status is to be detected by the change detect circuit, the Jumper A11 should be installed; if not, install A12. With A11, in the 0-to-1 transition can clock a 1 to IC1A-2 which will then reset IC1B. If a 1-to-0 transition of the point status is to be detected, then Jumper B11 should be installed; if not, install B12. With B11 in, a 1-to-0 transition at Terminal 3 becomes a 0-to-1 transition at IC1B-11 and causes a reset condition of IC1B.

Whenever a change is detected, Terminal D, $\overline{\text{CHG OCCD}}$ will be clamped low through a diode such as CR1. Terminal D's from other 66 LD/CD cards may be connected together to create a $\overline{\text{CHG OCCD}}$ signal buss which will be a logic 0 if any change in any card has occurred. The logic level at this new signal buss will remain low until all of the change detectors have been set. This buss should have a single 47K ohm pull-up resistor.

A second buss can be created by wiring together all of the $\overline{\text{GEN ALARM}}$'s at Terminal C. This buss requires its own 47K ohm pull up resistor. It will be low whenever a change detector is reset because of the clocking action at the flip-flop corresponding to IC18A. This second buss will stay low until a logic 1 is applied to Terminal 21, ARM GEN ALARM. Form B contacts may be used instead because of the pull up action of R21.

In actual practice the $\overline{\text{GEN ALARM}}$ buss can be connected to an audible alarm and the $\overline{\text{CHG OCCD}}$ buss can be wired to a visual display. In this manner an operator could reset the audible alarm immediately to prevent annoyance and yet still have an indication of change.

Change detection circuits may be simultaneously or individually set, or armed to detect the next change. To simultaneously arm all the detectors and to cancel flashing of all the status lamps, a logic 1 can be applied to Terminal 5 or a Form B contact can be opened because of the pull-up action of R8. To set, or arm, each point individually, a logic 1 (or opened Form B contact) is connected to the appropriate SLT-ACK terminal at the same time Terminal 14 is held high.

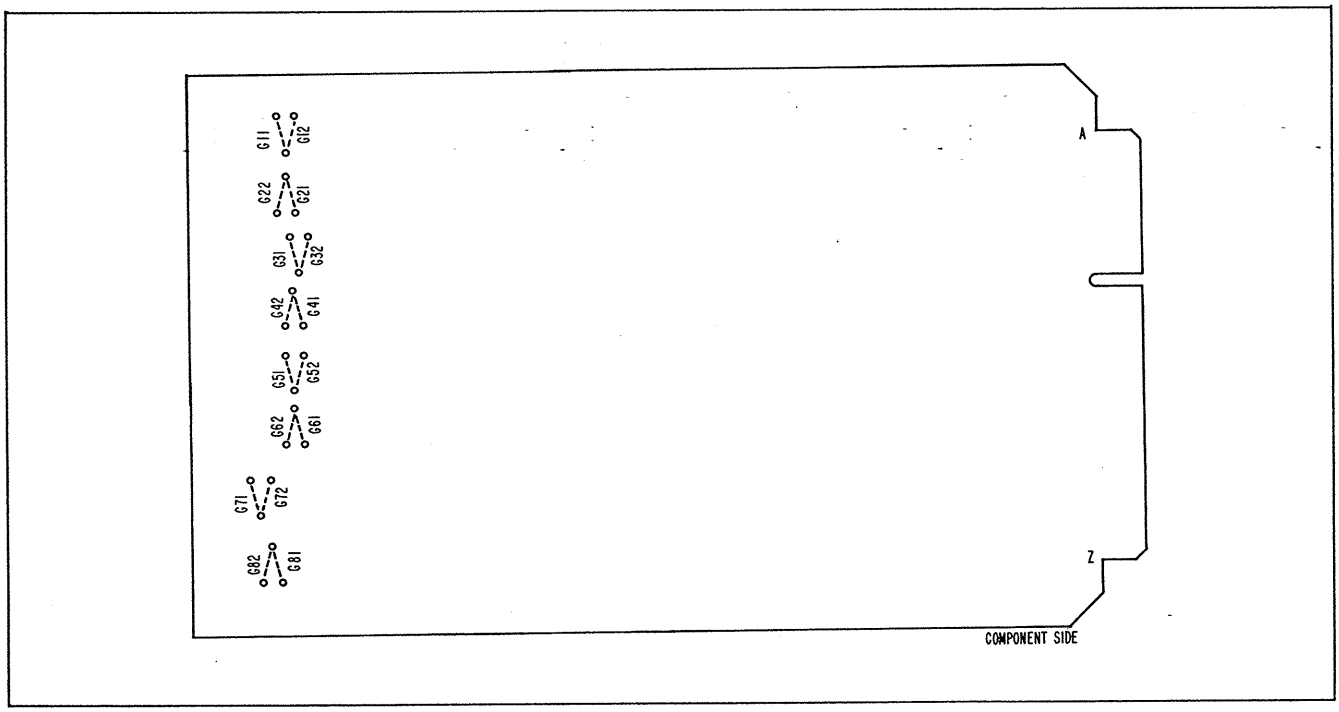


Figure 2. Location of jumpers for programming Model 66 LD.

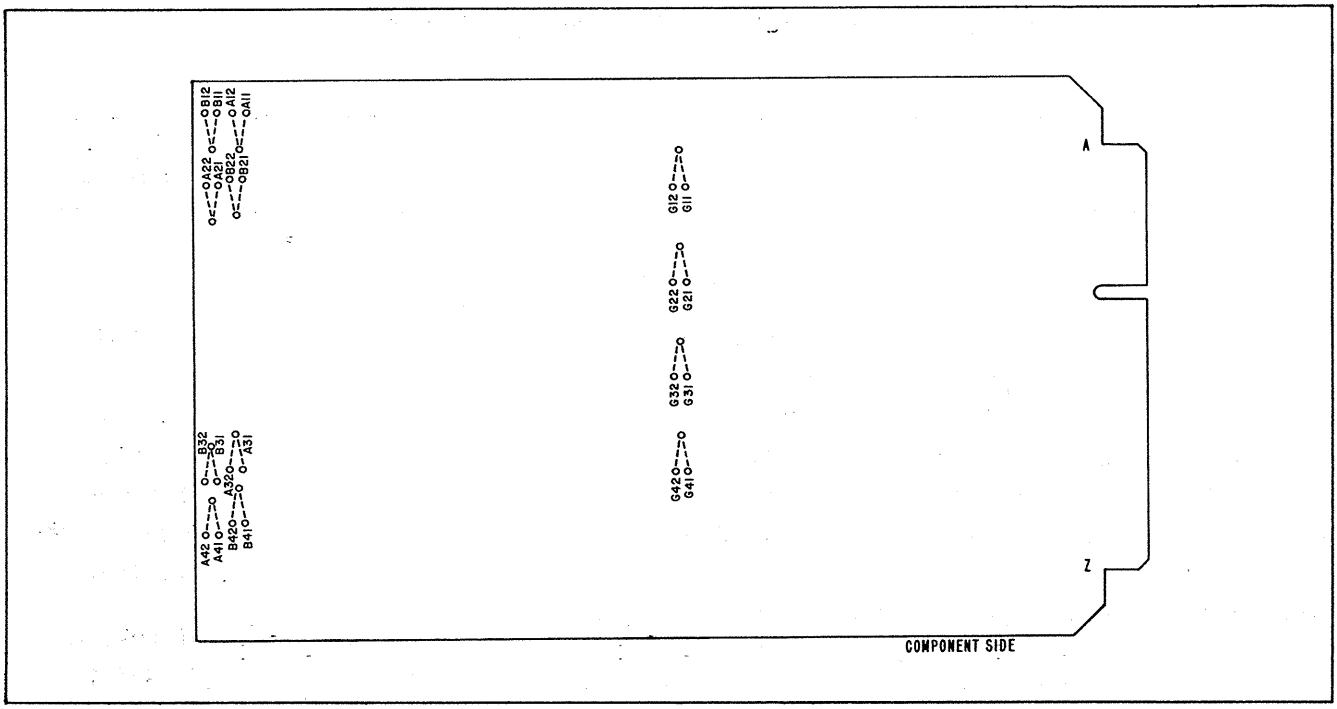
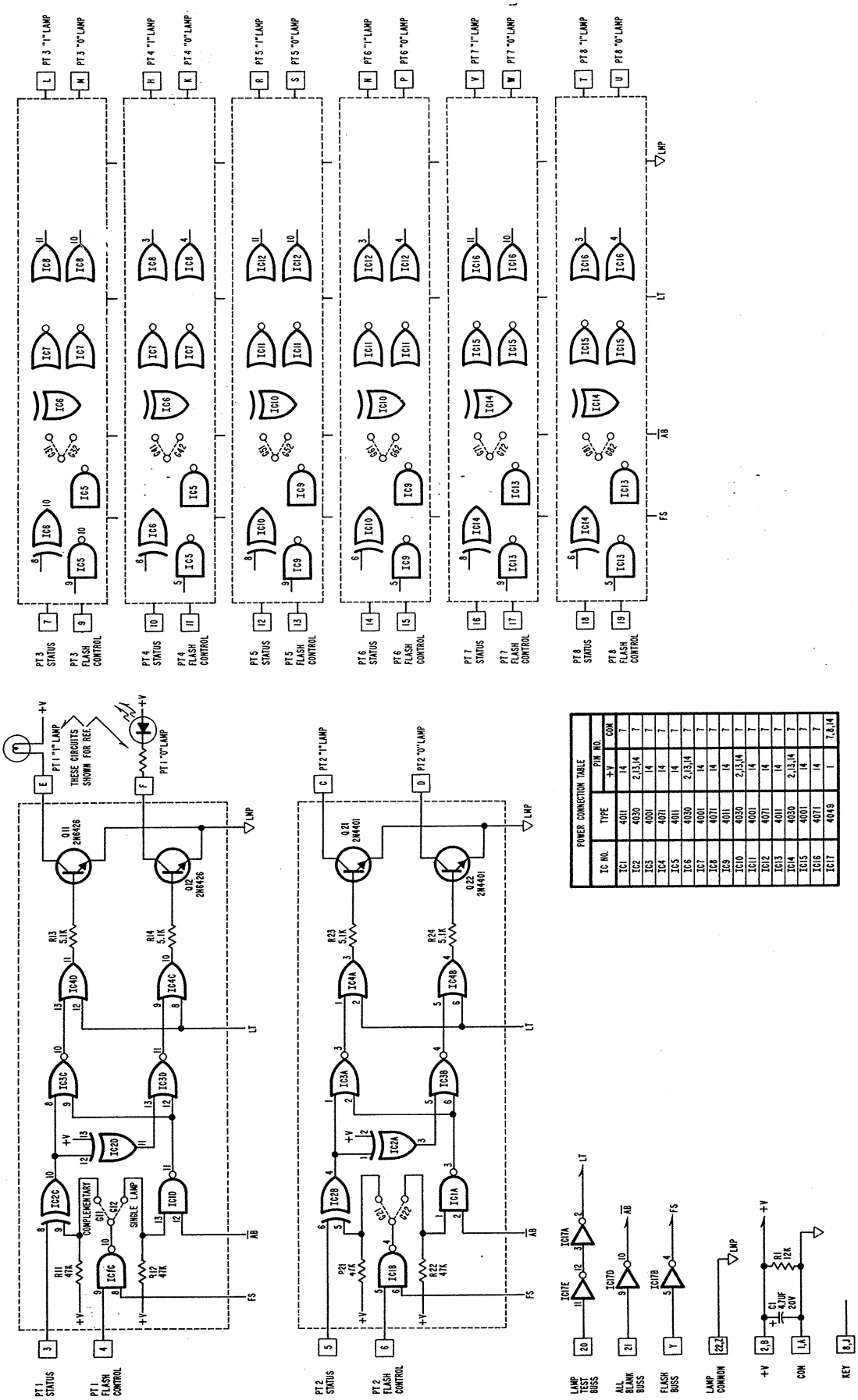


Figure 3. Location of jumpers for programming Model 66 LD/CD.

IC2B and IC2A serve to detect a change of status at Terminal 3 during the time when IC1A and 1B are being selectively armed. A 0-to-1 transition at Terminal 3 clocks a 1 to IC2B-12 and resets IC2A. Likewise, a 1-to-0 transition which is inverted by IC4F causes IC2A to clock a 0 to its output at pin 1. Thus any change at Terminal 3 will cause the $\overline{\text{SLTD COS}}$ output at Terminal K to be pulled low through CR2. This feature allows the card to be used to detect unauthorized change of state and cause flashing and alarming. However, during authorized change of status, the normal change detectors can be held in a set condition until the first change is detected via Terminal K. External logic can then be used to remove the logic 1 at Terminal 14, and thereafter have the card consider any additional changes at Terminal 3 as being unauthorized. Terminal K should have a single 47K ohm pull up resistor.

TABLE OF REPLACEABLE PARTS

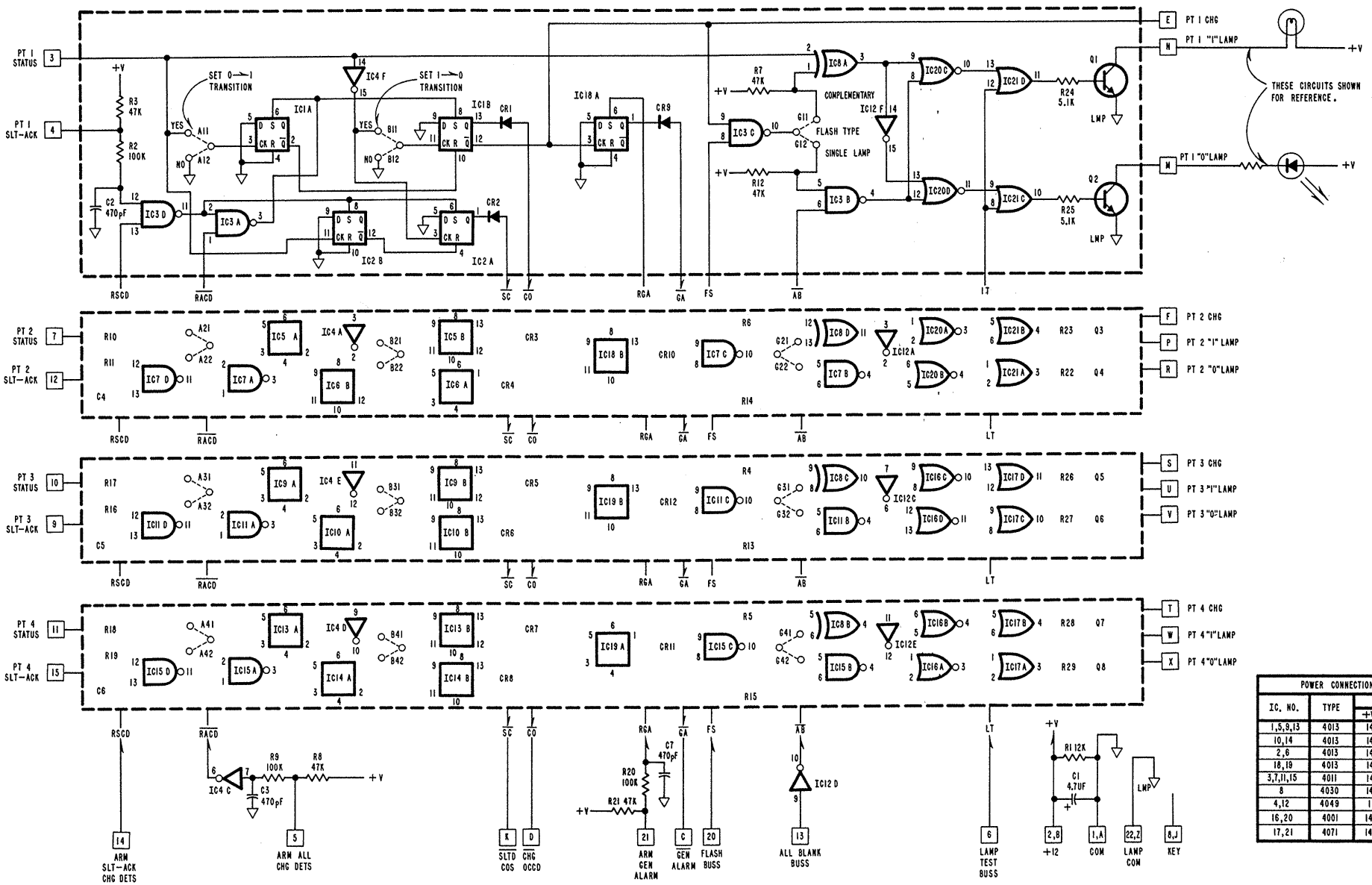
CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	8-Point Lamp Driver, Model 66 LD (Assembly HB-44550)	
C1	Capacitor, tantalum, 4.7 μF, 20%, 20 V, Kemet T324B475M020AS, or eq.	H-1007-711
IC1, 5, 9, 13	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC2, 6, 10, 14	Quad, EXCLUSIVE-OR gate, RCA CD4030AE, or eq.	H-0615-22
IC3, 7, 11, 15	Quad, 2-input NOR gate, RCA 4001AE, or eq.	H-0615-3
IC4, 8, 12, 16	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC17	Hex inverter buffer/converter, RCA CD4049AE, or eq.	H-0615-7
Q(1-8)1, (1-8)2	Transistor, Type 2N6426	HA-46531
R(1-8)1, (1-8)2 R(1-8)3, (1-8)4	Resistor, fixed, composition 5%, ¼ W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
———	Schematic	HE-44554
	4-Point Change Detect and Lamp Driver, Model 66 LD/CD (Assembly HB-44540)	
C1	Capacitor, tantalum 4.7 μF, 20%, 20 V, Kemet T324B475M020AS, or eq.	H-1007-711
C2 - 7	Capacitor, ceramic 470 pF, 10%, 100 V, Union Carbide CK12BX471-K, or eq.	H-1007-1358
CR1 - 12	Diode, Type 1N914B	HA-26482
IC1,2,5,6,9,10, 13, 14, 18, 19	Dual D-type flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC3, 7, 11, 15	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC4, 12	Hex inverter/buffer, RCA CD4049AE, or eq.	H-0615-7
IC8	Quad, EXCLUSIVE-OR gate, RCA CD4030AE, or eq.	H-0615-22
IC16, 20	Quad, 2-input NOR gate, RCA CD4011AE, or eq.	H-0615-3
IC17, 21	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
Q1 - 8	Transistor, Type 2N6426	HA-46531
R1 thru 29	Resistor, fixed, composition 5%, ¼ W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
———	Shorting bar	HA-42904
———	Schematic	HE-44544



POWER CONNECTION TABLE

IC NO.	TYPE	PIN NO. +V	PIN NO. COM
IC1	4011	14	7
IC2	4030	2,13,14	7
IC3	4001	14	7
IC4	4071	14	7
IC5	4011	14	7
IC6	4030	2,13,14	7
IC7	4001	14	7
IC8	4071	14	7
IC9	4011	14	7
IC10	4030	2,13,14	7
IC11	4001	14	7
IC12	4071	14	7
IC13	4011	14	7
IC14	4030	2,13,14	7
IC15	4001	14	7
IC16	4071	14	7
IC17	4049	1	7,8,14

Figure 4. Schematic of Circuit, Model 66 LD.



POWER CONNECTION TABLE			
IC. NO.	TYPE	PIN NO.	
		+V	COM
1,5,9,13	4013	14	4,5,7,9
10,14	4013	14	4,5,7,9
2,6	4013	14	5,7,9,10
18,19	4013	14	4,5,7,9,10
3,7,11,15	4011	14	7
8	4030	14	7
4,12	4049	1	5,8
16,20	4001	14	7
17,21	4071	14	7

Figure 5. Schematic of Circuit, Model 66 LD/CD.